

TSMC-02-066



February 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/600,393 06/20/03 |
Chi-Chun Chen et al.
METHOD OF FORMING DUAL GATE
INSULATOR
| _____ |

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.


The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
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P.O. Box 1450, Alexandria, VA 22313-1450, on February 9, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 2/9/04

TSMC-02-066

U.S. Patent 6,294,421 to Gonzalez et al., "Method of Fabricating Dual Gate Dielectric," discloses dual gate dielectric constructions and methods for different regions on an integrated circuit.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', with a long horizontal flourish extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

Aggregation Number

$$10 \overline{) 600,393}$$

Chi-Chun Chen et al.

06/20/03

Group Art Unit

(Use several sheets if necessary)

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion, Pages, Etc.)

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.